

hake
ci

- 5
10
15
20
25

C1
having the other end electrically connected to the other end of said first impurity storage region, and arranged in a direction different from the direction of arrangement of said first and second gate electrodes.

5 2. A semiconductor device as set forth in claim 1, wherein said first and second impurity storage regions are physically connected to each other by a semiconductor layer.

10 3. A semiconductor device as set forth in claim 1, wherein the other ends of said first and second impurity storage regions are electrically connected to each other through a conductive layer.

15 4. A semiconductor device as set forth in claim 1, wherein said first and second impurity storage regions are arranged in a direction perpendicular to the direction of arrangement of said first and second gate electrodes.

20 5. A semiconductor device as set forth in claim 1, wherein said first and second gate electrodes and said first and second impurity storage regions are formed in the same conductive semiconductor layer.

25 6. A semiconductor device as set forth in claim 1, wherein said element isolation region is buried in a trench formed a boundary between said first and second conductive type of element formation regions in a

semiconductor substrate.

7. A semiconductor device as set forth in claim
1, wherein said element isolation region isolates first
and second element formation regions comprised of
5 semiconductor layers formed on an insulation layer.

8. A semiconductor device as set forth in claim
7, wherein said element isolation region is buried in a
trench formed in said semiconductor layers.

10 *hank*
co 2. A semiconductor device as set forth in claim
2, wherein:

said semiconductor layer is formed by
polycrystalline silicon and

15 said first and second gate electrodes and
first and second impurity storage regions are formed by
selectively implanting impurities to said
polycrystalline silicon layer.

20 10. A semiconductor device as set forth in claim
2, wherein the width of said semiconductor layer
physically connecting said first and second impurity
storage regions is a value allowing mask misalignment
when forming said first and second gate electrodes and
first and second impurity storage regions.

11. A semiconductor device as set forth in claim
1, wherein:

25 the widths of said first and second impurity

storage regions are equal to the gate length of said first and second gate electrodes and

the lengths of said first and second impurity storage regions are longer than said gate length.